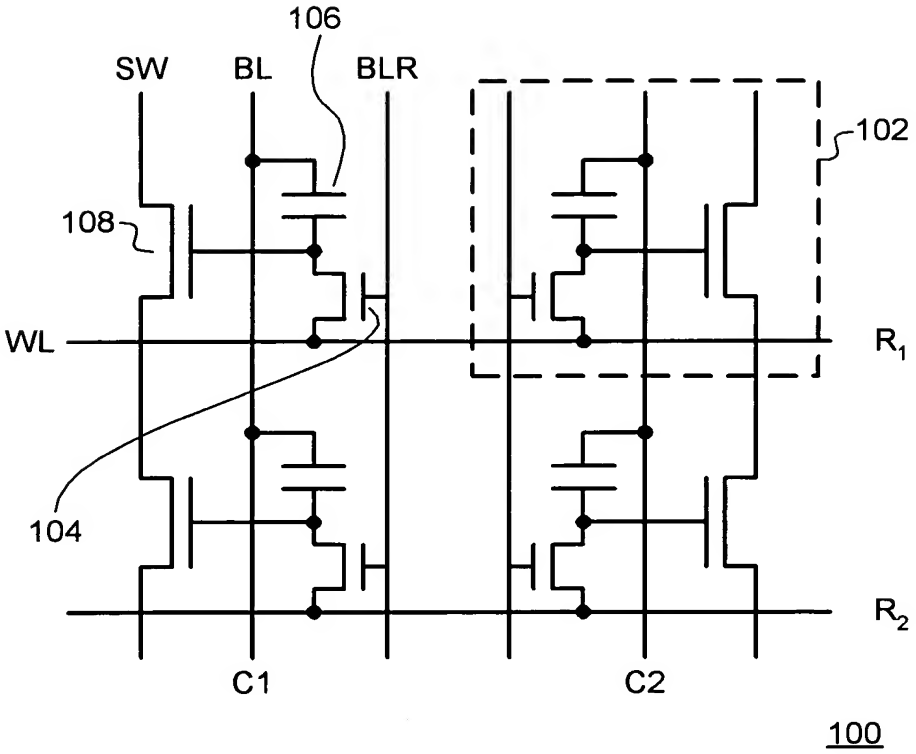

FIGURE 1

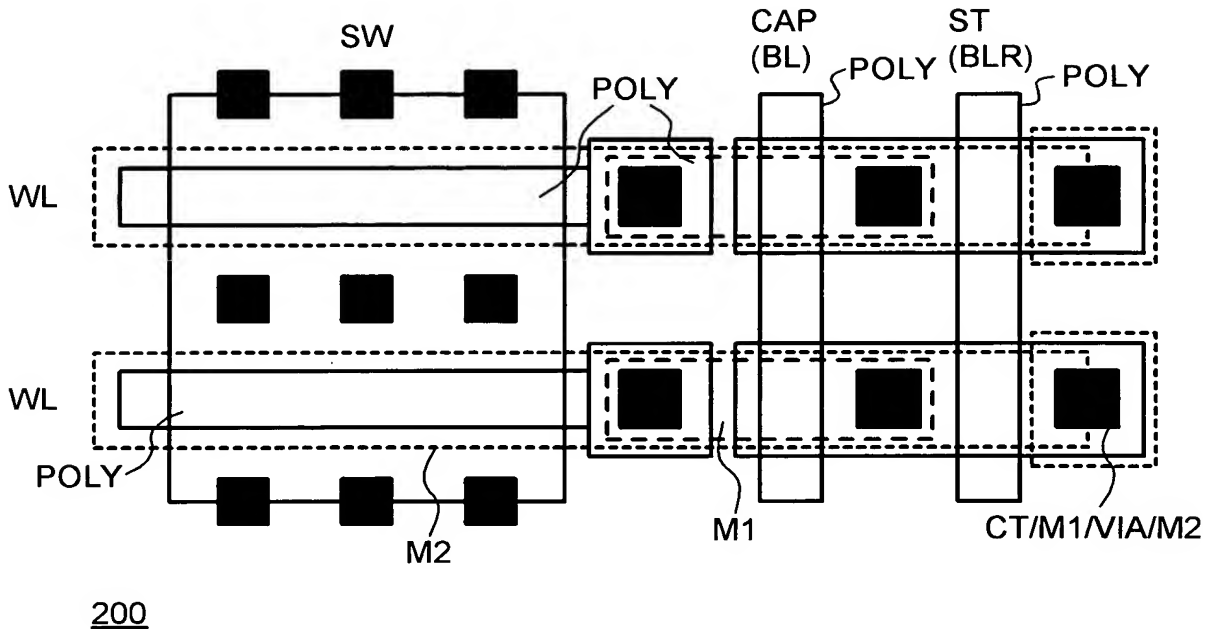

FIGURE 2

0.18um LV XPM FPGA CELL OPERATION

		VBL	VBLR	VWL			PROGRAM	
PROGRAM	SC/SR	8	3.3	0			YES	301
	SC/UR	8	3.3	3.3			NO	303
	UC/SR	0	0	0			NO	305
	UC/UR	0	0	3.3			NO	307
							SENSE CURRENT	
READ	SC/SR	1.8 - 3.3	1.8	0			YES	309
	SC/UR	1.8 - 3.3	1.8	1.8			NO	311
	UC/SR	0	0	0			NO	313
	UC/UR	0	0	1.8			NO	315
OPERATION		1.8	0 - 0.8	0				317

FIGURE 3

0.18um IO XPM FPGA CELL OPERATION

		VBL	VBR	VWL			PROGRAM	
PROGRAM	SC/SR	8	3.3	0			YES	401
	SC/UR	8	3.3	3.3			NO	403
	UC/SR	0	0	0			NO	405
	UC/UR	0	0	3.3			NO	407
							SENSE CURRENT	
READ	SC/SR	3.3	3.3	0			YES	409
	SC/UR	3.3	3.3	3.3			NO	411
	UC/SR	0	0	0			NO	413
	UC/UR	0	0	3.3			NO	415
OPERATION		3.3	0.3 - 0.8	0			YES	417

FIGURE 4

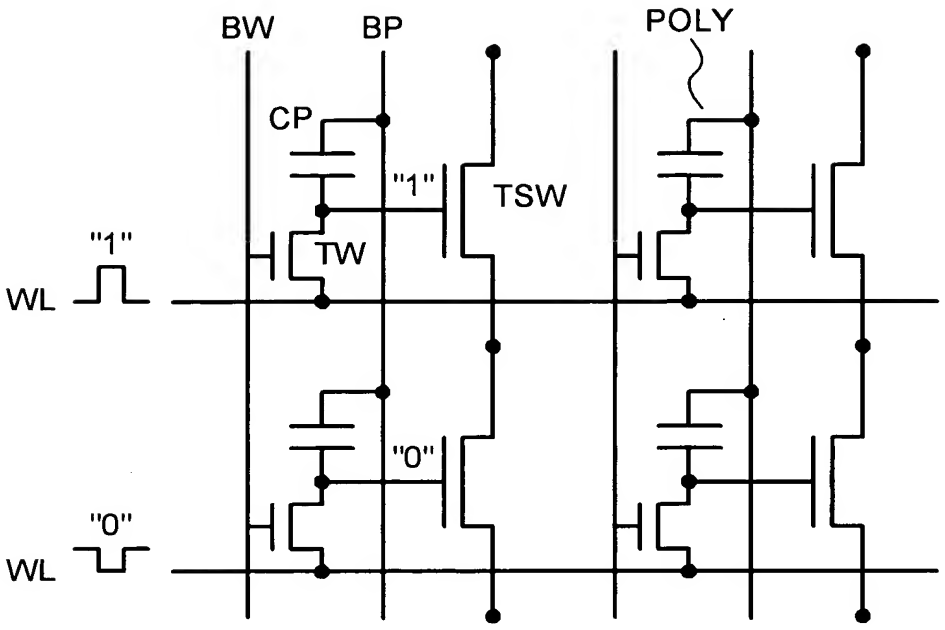

FIGURE 5

DYNAMIC XPM FPGA CELL OPERATION

		VBW	VBP	VWL(1)	VWL(0)
WRITE OR REFRESHING BY COLUMNS	SC	V_{cc}	0	V_{cc}	0
	UC	0	0	V_{cc}	0

*SC-SELECTED COLUMN; UC-UNSELECTED COLUMN

FIGURE 6

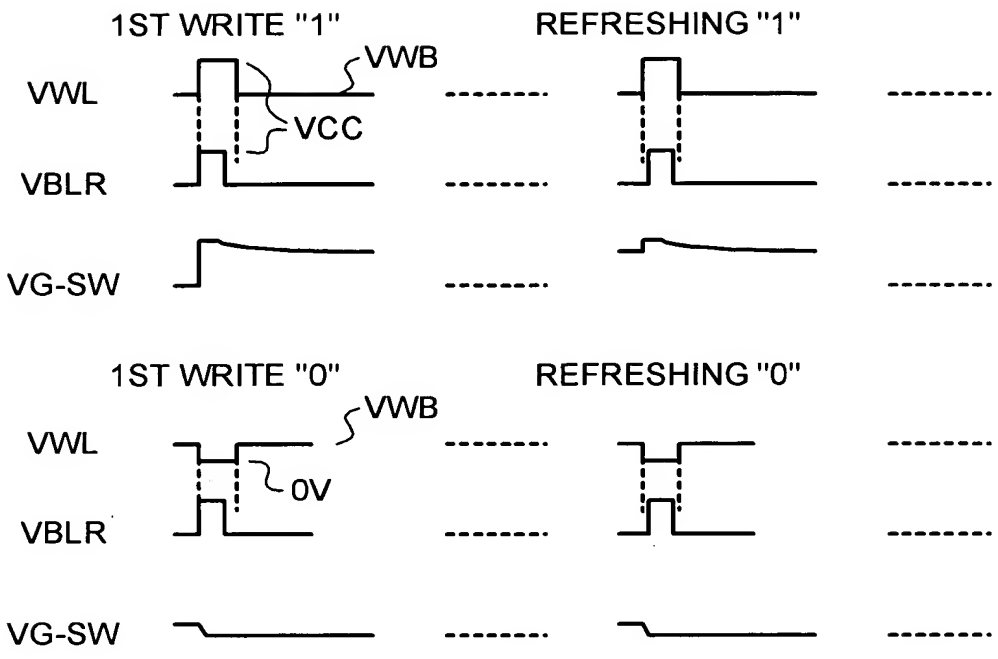
1ST WRITE "1"
REFRESHING "1"
VWB
VWL
VCC
VBLR
VG-SW
1ST WRITE "0"
REFRESHING "0"
VWB
VWL
0V
VBLR
VG-SW

FIGURE 7

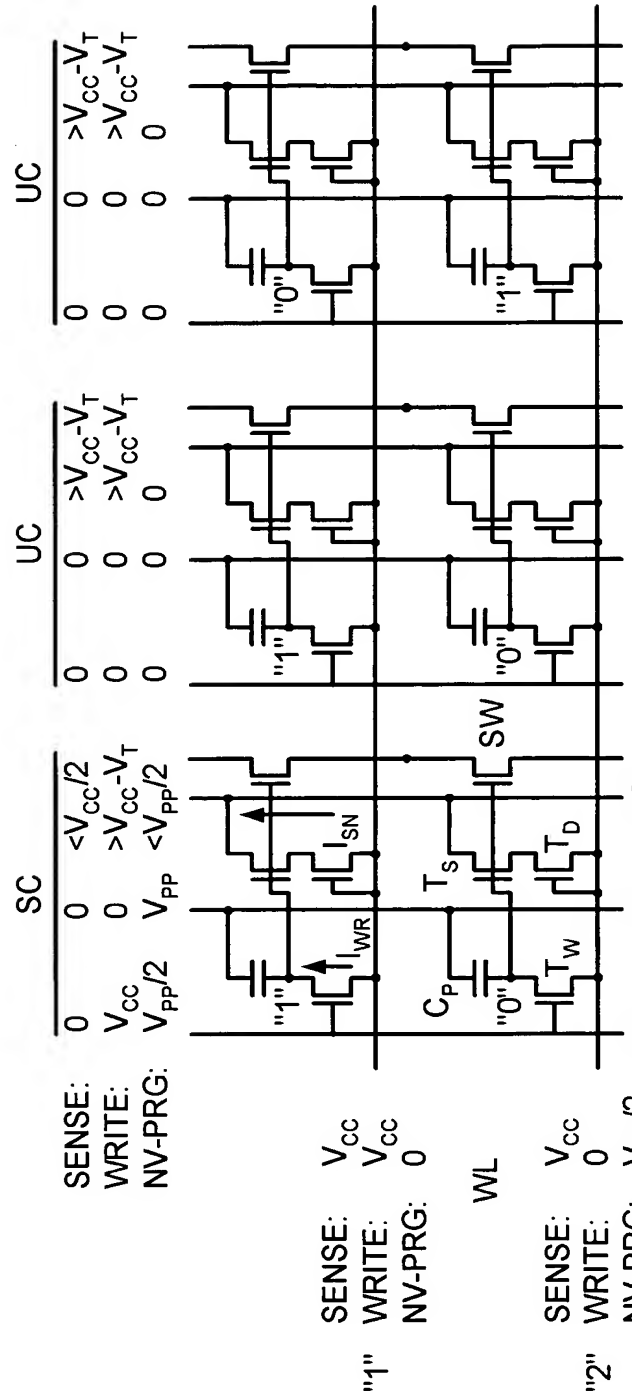
SC
UC
UC
UC
SENSE:
WRITE:
NV-PRG:
"1"
"0"
"0"
"1"
"1"
"0"
"0"
"1"
I_{WR}
I_{SN}
C_P
T_S
T_W
T_D
SW
BW
BP
BS
WL
"1"
"2"
SENSE: V_{CC}
WRITE: V_{CC}
NV-PRG: 0
SENSE: V_{CC}
WRITE: 0
NV-PRG: $V_{PP}/2$
0
V_{CC}
$V_{PP}/2$
V_{PP}
$<V_{CC}/2$
$>V_{CC}-V_T$
$<V_{PP}/2$
$>V_{CC}-V_T$

FIGURE 8

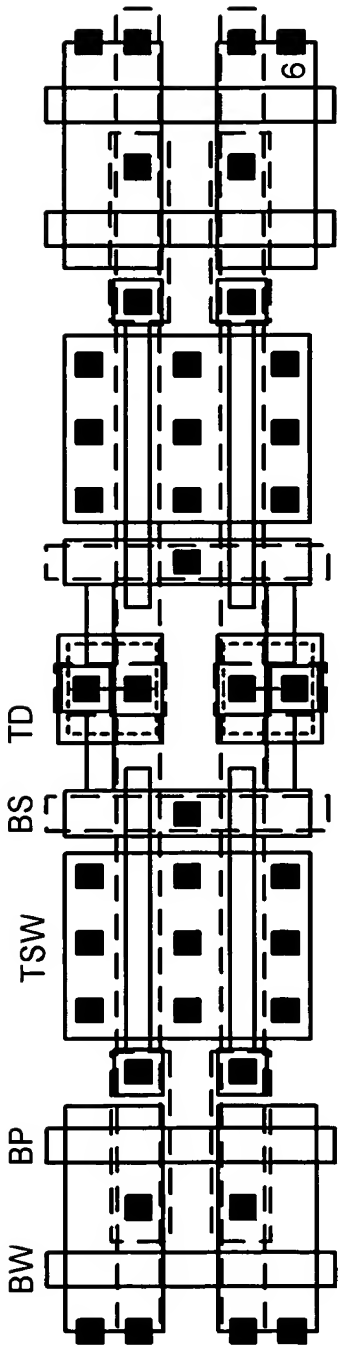

FIGURE 9

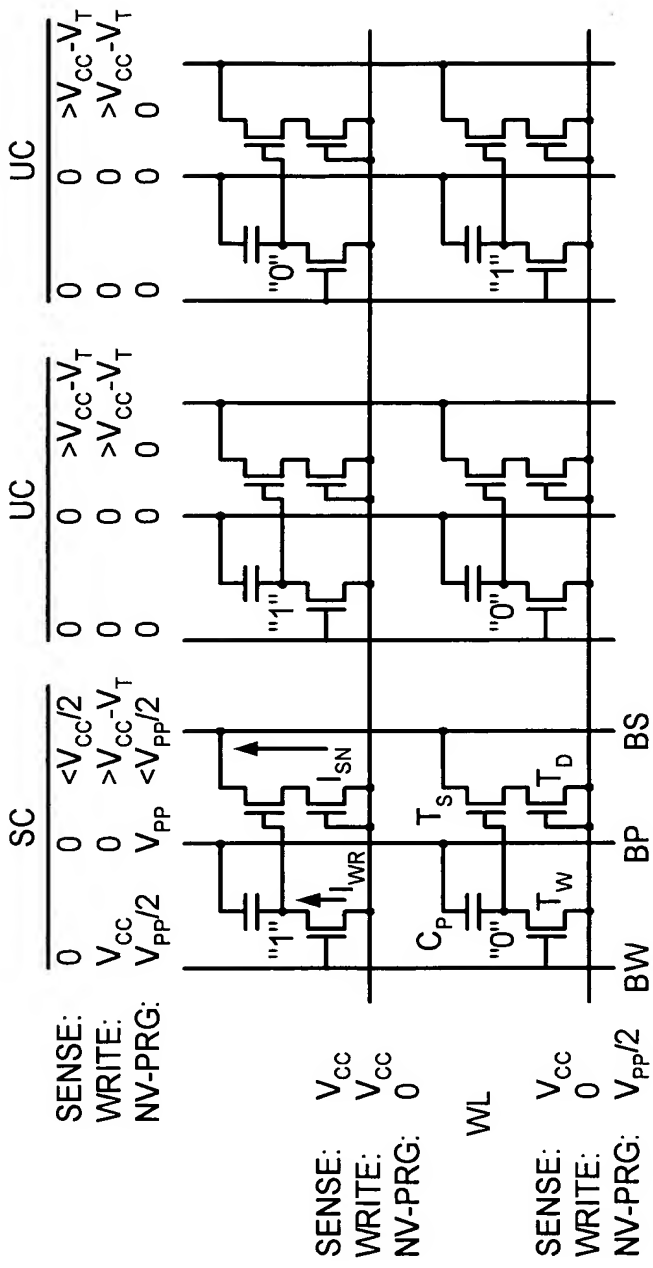
SC
UC
UC
SENSE:
WRITE:
NV-PRG:
0
V_{CC}
$V_{PP}/2$
0
0
V_{PP}
0
$<V_{CC}/2$
$>V_{CC}-V_T$
$<V_{PP}/2$
0
0
0
$>V_{CC}-V_T$
$>V_{CC}-V_T$
0
0
0
"1"
"0"
"1"
"0"
"0"
"1"
I_{WR}
I_{SN}
C_P
T_S
T_W
T_D
BW
BP
BS
WL
SENSE: V_{CC}
WRITE: V_{CC}
NV-PRG: 0
SENSE: V_{CC}
WRITE: 0
NV-PRG: $V_{PP}/2$

FIGURE 10

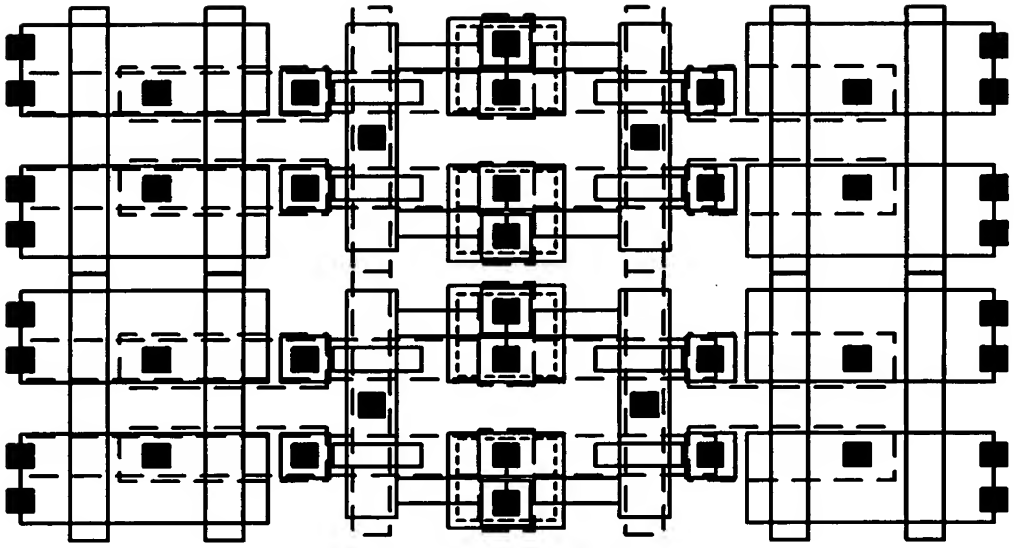

FIGURE 11